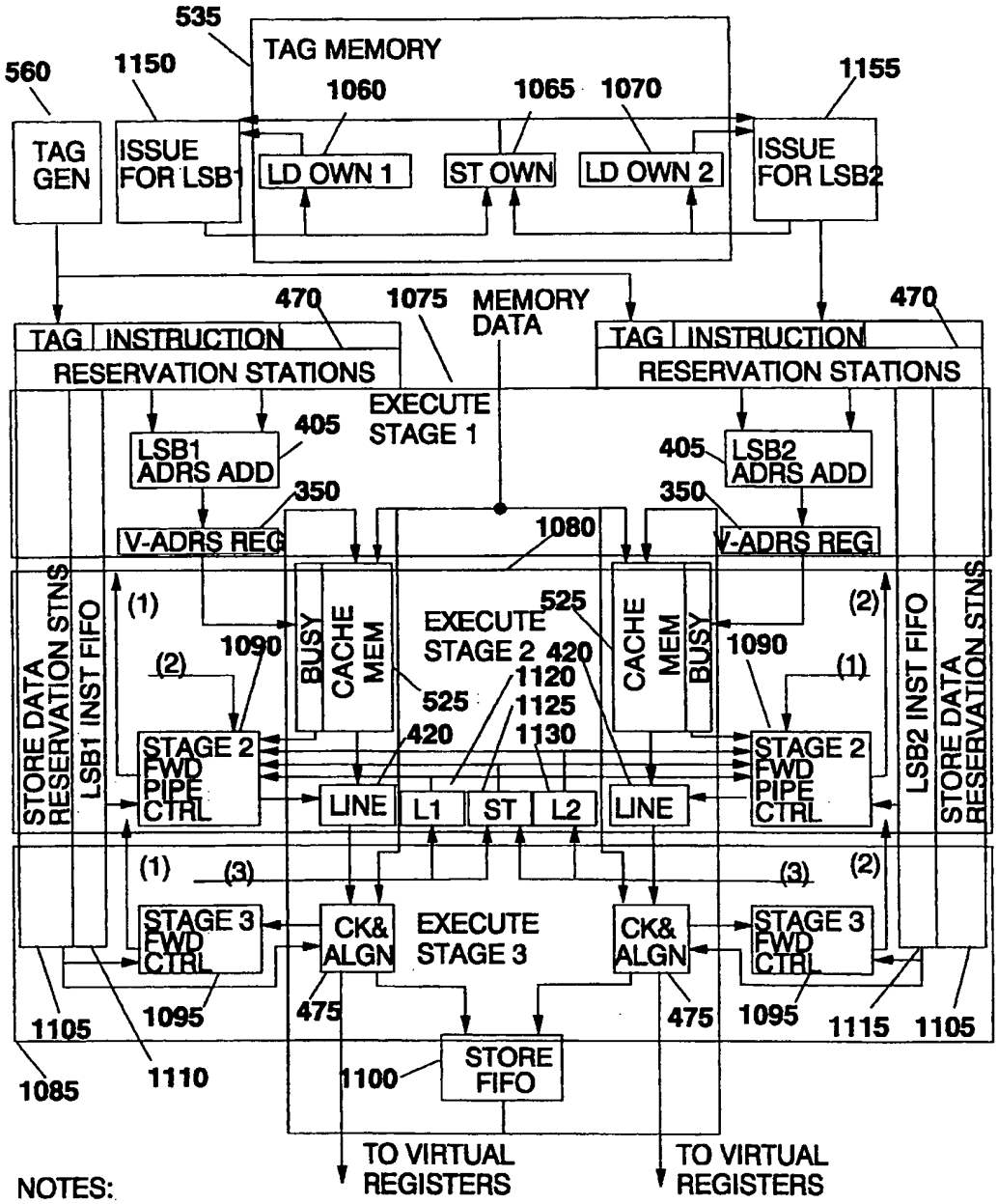
	L #	Hits	Search Text	DBs
1	L1	2862	((indicat$3 flag tag bit field mode) near10 ((utiliz$3 us$3 enabl$3 disabl$3 prohibit$3 inhibit$3 activ$5 deactiv$5) near10 prediction))	USPAT; US-PGPUB
2	L4	838	prediction near10 (effective ineffective reliab$5 low confidence hard difficult acccura$3 inaccura$3) and 1	USPAT; US-PGPUB
3	L5	102	4 and (branch and prediction).ab,ti.	USPAT; US-PGPUB

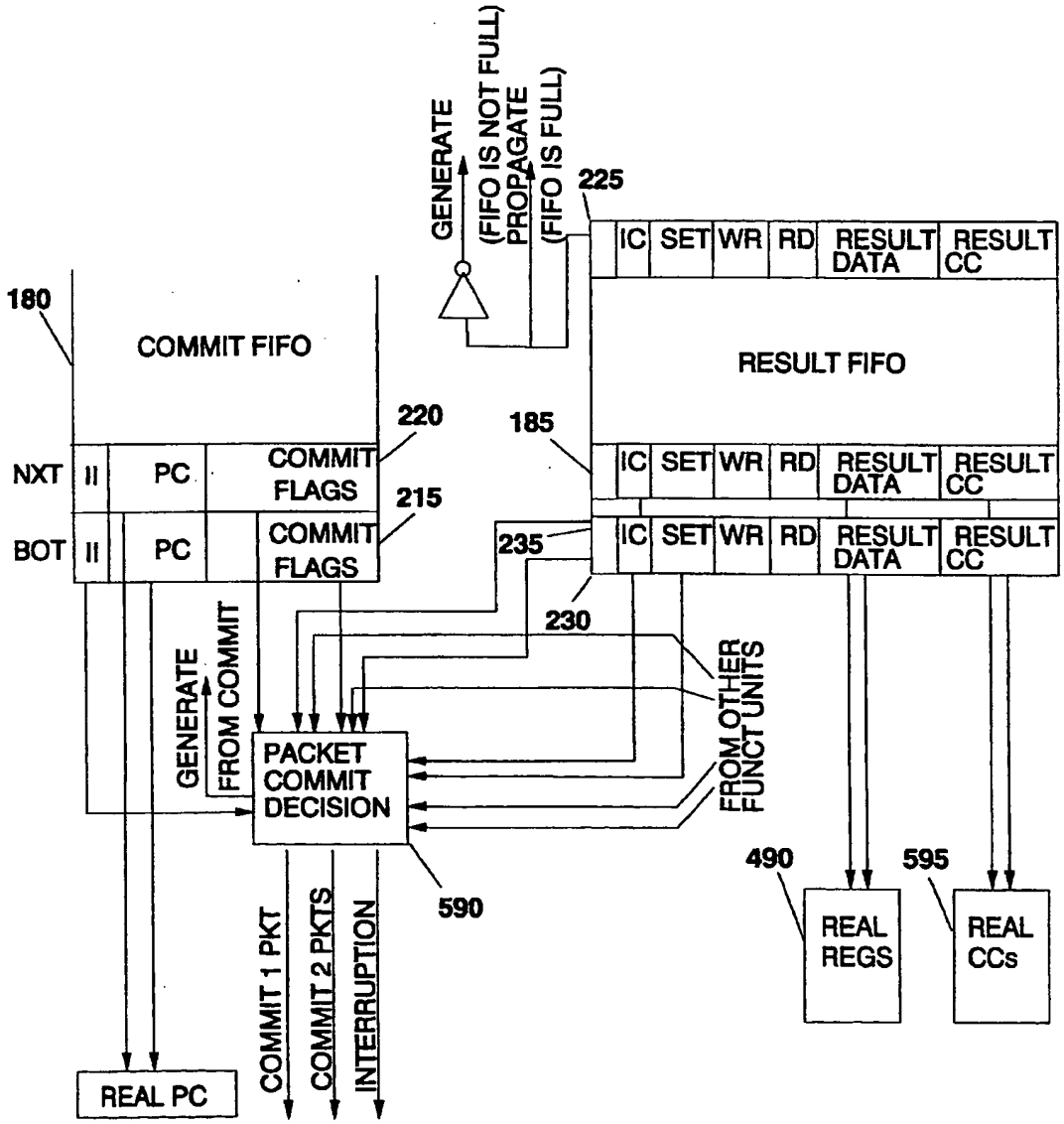
Figure 27e. Invention,
Dynamic Scheduling Embodiment,
Main Memory Tagging



NOTES:
(1) GENERATE & PROPAGATE
(2) PREVIOUS OWNER TAG(S) FROM INST
(3) TAG FROM THE INSTRUCTION

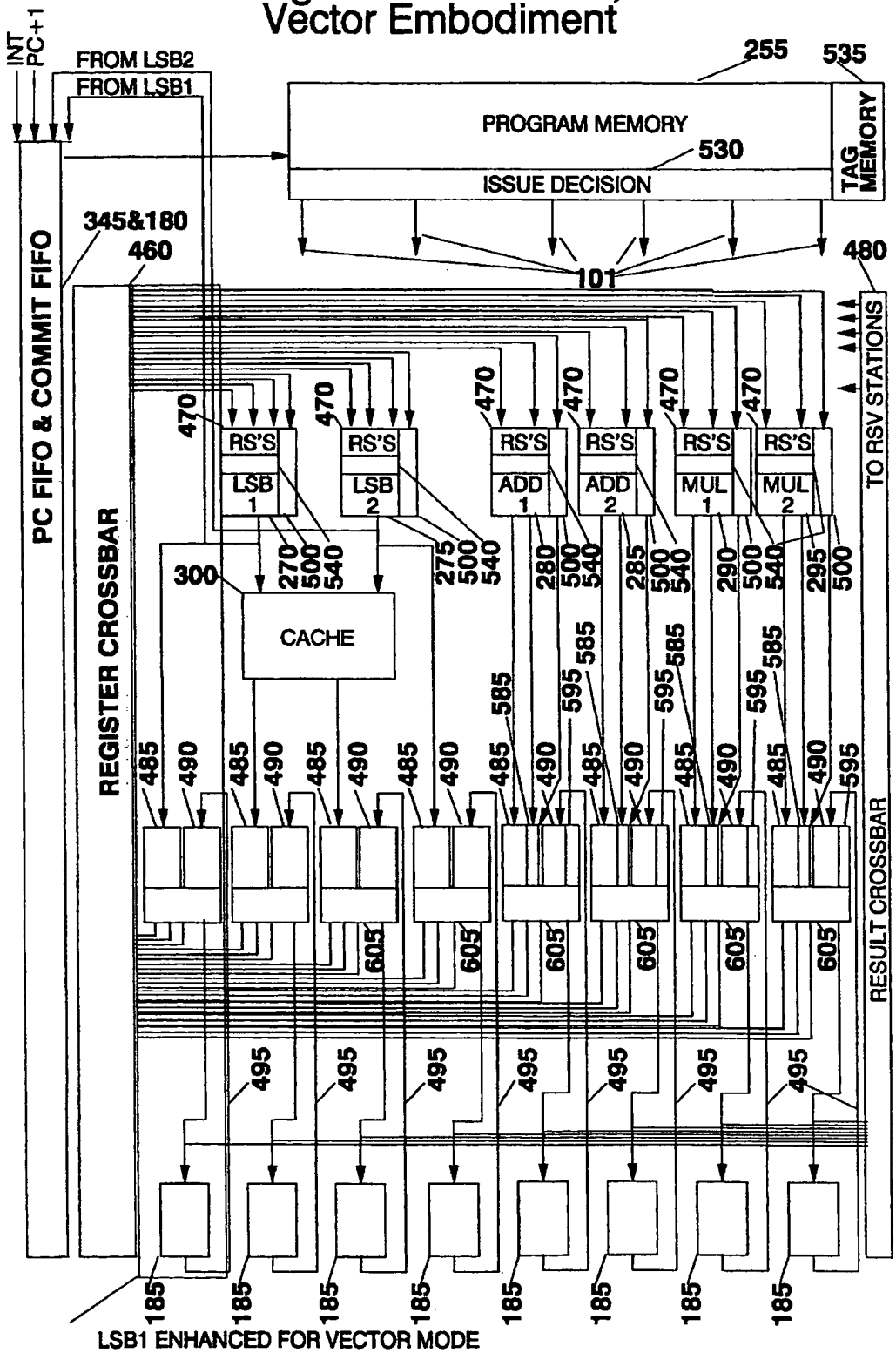
	Document ID	U	Title	Current OR
1	US 20040030838 A1	☐	Instruction cache way prediction for jump targets	711/137
2	US 20030084271 A1	☒	Speculative execution for java hardware accelerator	712/209
3	US 20030065912 A1	☒	Removing redundant information in hybrid branch prediction	712/239
4	US 20030041230 A1	☒	METHOD AND SYSTEM FOR BRANCH TARGET PREDICTION USING PATH INFORMATION	712/238
5	US 20020194464 A1	☒	Speculative branch target address cache with selective override by seconday predictor based on branch instruction type	712/239
6	US 20020194463 A1	☒	Speculative hybrid branch direction predictor	712/239
7	US 20020194462 A1	☒	Apparatus and method for selecting one of multiple target addresses stored in a speculative branch target address cache per instruction cache line	712/238
8	US 20020194461 A1	☒	Speculative branch target address cache	712/238
9	US 20020188833 A1	☒	Dual call/return stack branch prediction system	712/236
10	US 20020138236 A1	☒	Processor having execution result prediction function for instruction	702/186
11	US 20020078332 A1	☒	Conflict free parallel read access to a bank interleaved branch predictor in a processor	712/240
12	US 20020073301 A1	☒	Hardware for use with compiler generated branch information	712/235
13	US 20020029333 A1	☒	Methods and apparatus for branch prediction using hybrid history with index sharing	712/239
14	US 20010047467 A1	☒	METHOD AND APPARATUS FOR BRANCH PREDICTION USING FIRST AND SECOND LEVEL BRANCH PREDICTION TABLES	712/228
15	US 20010037446 A1	☒	Processor and branch prediction method	712/239
16	US 20010032309 A1	☒	Static branch prediction mechanism for conditional branch instructions	712/239
17	US 20010020267 A1	☒	Pipeline processing apparatus with improved efficiency of branch prediction, and method therefor	712/239

Figure 27f. Invention,
Real Registers and CCs,
Dynamic Scheduling Embodiment



	Document ID	U	Title	Current OR
18	US 20010 01690 3 A1	☒	Software branch prediction filtering for a microprocessor	712/239
19	US 20010 01134 6 A1	☒	Branch prediction method, arithmetic and logic unit, and information processing apparatus	712/239
20	US 66786 38 B2	☒	Processor having execution result prediction function for instruction	702/186
21	US 66623 60 B1	☒	Method and system for software control of hardware branch prediction mechanism in a data processor	717/131
22	US 66622 95 B2	☒	Method and system dynamically presenting the branch target address in conditional branch instruction	712/234
23	US 66402 98 B1	☒	Branch prediction apparatus	712/239
24	US 66011 61 B2	☒	Method and system for branch target prediction using path information	712/238
25	US 65981 52 B1	☒	Increasing the overall prediction accuracy for multi-cycle branch prediction and apparatus by enabling quick recovery	712/228
26	US 65713 31 B2	☒	Static branch prediction mechanism for conditional branch instructions	712/239
27	US 65534 88 B2	☒	Method and apparatus for branch prediction using first and second level branch prediction tables	712/239
28	US 65105 11 B2	☒	Methods and apparatus for branch prediction using hybrid history with index sharing	712/240
29	US 65021 88 B1	☒	Dynamic classification of conditional branches in global history branch prediction	712/234
30	US 64991 01 B1	☒	Static branch prediction mechanism for conditional branch instructions	712/239
31	US 64272 06 B1	☒	Optimized branch predictions for strongly predicted compiler branches	712/239
32	US 64250 75 B1	☒	Branch prediction device with two levels of branch prediction cache	712/239
33	US 63857 20 B1	☒	Branch prediction method and processor using origin information, relative position information and history information	712/240
34	US 63743 51 B1	☒	Software branch prediction filtering for a microprocessor	712/239
35	US 63413 48 B1	☒	Software branch prediction filtering for a microprocessor	712/239
36	US 63321 90 B1	☒	Branch prediction method using a prediction table indexed by fetch-block address	712/240
37	US 62826 29 B1	☒	Pipelined processor for performing parallel instruction recording and register assigning	712/23
38	US 62791 07 B1	☒	Branch selectors associated with byte ranges within an instruction cache for rapidly identifying branch predictions	712/239
39	US 62726 24 B1	☒	Method and apparatus for predicting multiple conditional branches	712/239

Figure 28. Invention, Vector Embodiment



	Document ID	U	Title	Current OR
40	US 6272623 B1	☒	Methods and apparatus for branch prediction using hybrid history with index sharing	712/239
41	US 6269436 B1	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
42	US 6253316 B1	☒	Three state branch history using one bit in a branch prediction mechanism	712/239
43	US 6247123 B1	☒	Branch prediction mechanism employing branch selectors to select a branch prediction	712/239
44	US 6247122 B1	☒	Method and apparatus for performing branch prediction combining static and dynamic branch predictors	712/239
45	US 6233679 B1	☒	Method and system for branch prediction	712/240
46	US 6178498 B1	☒	Storing predicted branch target address in different storage according to importance hint in branch prediction instruction	712/239
47	US 6170053 B1	☒	Microprocessor with circuits, systems and methods for responding to branch instructions based on history of prediction accuracy	712/240
48	US 6157999 A	☒	Data processing system having a synchronizing link stack and method thereof	712/243
49	US 6141748 A	☒	Branch selectors associated with byte ranges within an instruction cache for rapidly identifying branch predictions	712/239
50	US 6108774 A	☒	Branch prediction with added selector bits to increase branch prediction capacity and flexibility with minimal added bits	712/240
51	US 6081887 A	☒	System for passing an index value with each prediction in forward direction to enable truth predictor to associate truth value with particular branch instruction	712/239
52	US 6067616 A	☒	Branch prediction device with two levels of branch prediction cache	712/239
53	US 6055629 A	☒	Predicting for all branch instructions in a bunch based on history register updated once for all of any taken branches in a bunch	712/239
54	US 6052776 A	☒	Branch operation system where instructions are queued until preparations is ascertained to be completed and branch distance is considered as an execution condition	712/233
55	US 6029228 A	☒	Data prefetching of a load target buffer for post-branch instructions based on past prediction accuracy's of branch predictions	711/137
56	US 6016545 A	☒	Reduced size storage apparatus for storing cache-line-related data in a high frequency microprocessor	712/238
57	US 6014734 A	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
58	US 5995749 A	☒	Branch prediction mechanism employing branch selectors to select a branch prediction	712/239
59	US 5983335 A	☒	Computer system having organization for multiple condition code setting and for testing instruction out-of-order	712/23
60	US 5978906 A	☒	Branch selectors associated with byte ranges within an instruction cache for rapidly identifying branch predictions	712/239
61	US 5974542 A	☒	Branch prediction unit which approximates a larger number of branch predictions using a smaller number of branch predictions and an alternate target indication	712/239
62	US 5961638 A	☒	Branch prediction mechanism employing branch selectors to select a branch prediction	712/239

Figure 29. Invention, One-Packet Vector Loop Example

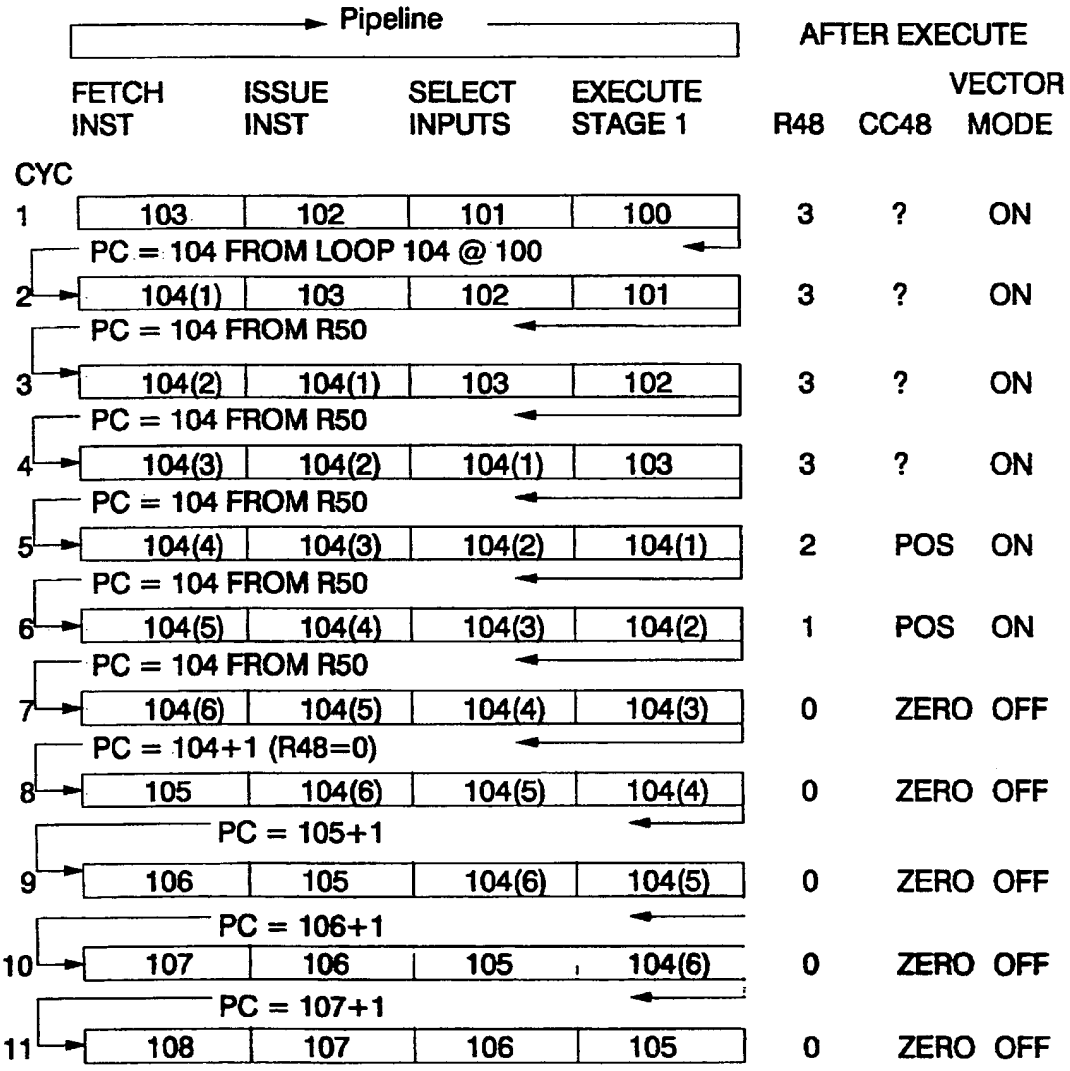
R48 = 6-3 R49 = 104 R50 = 104

ADDRS	LSB1 INST	LSB2 INST
100	LOOP 104	STORE RK,RA,1,IRA
101	ANY	STORE RK,RA,1,IRA
102	ANY	STORE RK,RA,1,IRA
103	ANY	STORE RK,RA,1,IRA
104	DEC/SET	STORE RK,RA,1,IRA
105	ANY	ANY
106	ANY	ANY
107	ANY	ANY

STORE TO 4 LOCATIONS (OUTSIDE THE LOOP)

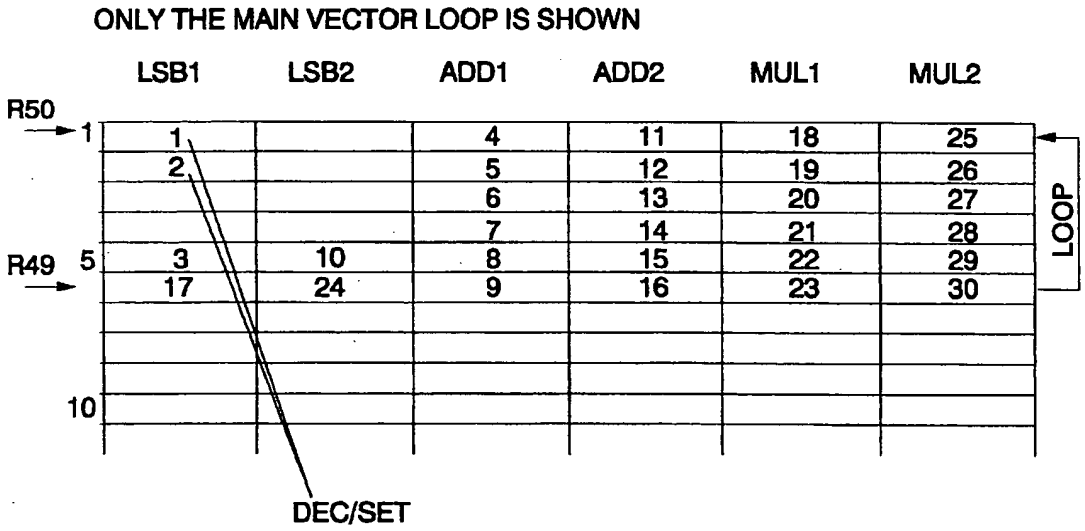
STORE TO 6 LOCATIONS (INSIDE THE LOOP)

TOTAL OF 10 LOCATIONS



	Document ID	U	Title	Current OR
63	US 5954816 A	☒	Branch selector prediction	712/239
64	US 5949995 A	☒	Programmable branch prediction system and method for inserting prediction operation which is independent of execution of program code	712/239
65	US 5935241 A	☒	Multiple global pattern history tables for branch prediction in a microprocessor	712/240
66	US 5933860 A	☒	Multiprobe instruction cache with instruction-based probe hint generation and training whereby the cache bank or way to be accessed next is predicted	711/213
67	US 5928358 A	☒	Information processing apparatus which accurately predicts whether a branch is taken for a conditional branch instruction, using small-scale hardware	712/239
68	US 5901307 A	☒	Processor having a selectively configurable branch prediction unit that can access a branch prediction utilizing bits derived from a plurality of sources	712/240
69	US 5896529 A	☒	Branch prediction based on correlation between sets of bunches of branch instructions	712/239
70	US 5881308 A	☒	Computer organization for multiple and out-of-order execution of condition code testing and setting instructions out-of-order	712/23
71	US 5881278 A	☒	Return address prediction system which adjusts the contents of return stack storage to enable continued prediction after a mispredicted branch	712/242
72	US 5875325 A	☒	Processor having reduced branch history table size through global branch history compression and method of branch prediction utilizing compressed global branch history	712/240
73	US 5864707 A	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
74	US 5864697 A	☒	Microprocessor using combined actual and speculative branch history prediction	712/240
75	US 5848269 A	☒	Branch predicting mechanism for enhancing accuracy in branch prediction by reference to data	712/239
76	US 5835754 A	☒	Branch prediction system for superscalar processor	712/239
77	US 5835745 A	☒	Hardware instruction scheduler for short execution unit latencies	712/215
78	US 5828874 A	☒	Past-history filtered branch prediction	712/240
79	US 5822575 A	☒	Branch prediction storage for storing branch prediction information such that a corresponding tag may be routed with the branch instruction	712/239
80	US 5794028 A	☒	Shared branch prediction structure	712/240
81	US 5740415 A	☒	Instruction supplying apparatus with a branch target buffer having the contents so updated as to enhance branch prediction accuracy	712/238
82	US 5729707 A	☒	Instruction prefetch circuit and cache device with branch detection	712/207
83	US 5687360 A	☒	Branch predictor using multiple prediction heuristics and a heuristic identifier in the branch instruction	712/240
84	US 5649137 A	☒	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/207
85	US 5630157 A	☒	Computer organization for multiple and out-of-order execution of condition code testing and setting instructions	712/23

Figure 30. Invention,
LFK24 Main Loop Mapping,
Vector Embodiment



	Document ID	U	Title	Current OR
86	US 5619662 A	☒	Memory reference tagging	712/216
87	US 5581719 A	☒	Multiple block line prediction	712/207
88	US 5577217 A	☒	Method and apparatus for a branch target buffer with shared branch pattern tables for associated branch predictions	712/200
89	US 5564118 A	☒	Past-history filtered branch prediction	712/240
90	US 5553255 A	☒	Data processor with programmable levels of speculative instruction fetching and method of operation	712/235
91	US 5553253 A	☒	Correlation-based branch prediction in digital computers	712/240
92	US 5519841 A	☒	Multi instruction register mapper	711/202
93	US 5515518 A	☒	Two-level branch prediction cache	712/239
94	US 5511175 A	☒	Method an apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/216
95	US 5381533 A	☒	Dynamic flow instruction cache memory organized around trace segments independent of virtual address line	712/215
96	US 5327547 A	☒	Two-level branch prediction cache	711/137
97	US 5313634 A	☒	Computer system branch prediction of subroutine returns	712/240
98	US 5226130 A	☒	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/238
99	US 5163140 A	☒	Two-level branch prediction cache	711/140
100	US 5142634 A	☒	Branch prediction	712/240
101	US 5093778 A	☒	Integrated single structure branch prediction cache	712/240
102	US 4430706 A	☐	Branch prediction apparatus and method for a data processing system	712/237

Figure 31a. Invention,

IBM 370-XA CISC Embodiment